Content-Aware Write Reduction Mechanism of Phase-Change RAM based Frame Store in H.264 Video Codec System

Sanchuan Guo, Zhenyu Liu, Guohong Li and Dongsheng Wang
Tsinghua National Laboratory for Information Science and Technology
Department of Computer Science and Technology, Tsinghua University
Beijing 100084, China
Email: {guosc07,ligh08}@mails.tsinghua.edu.cn, {liuzhenyu73,wds}@mail.tsinghua.edu.cn

***Abstract*— H.264 video codec system requires big capacity of Frame Store (FS) for buffering reference frames. The up-to-date Phase-change Random Access Memory (PRAM) is the promising approach for on-chip caching the reference signals, as PRAM offers the advantages in terms of high density and low leakage power. However, the write endurance problem, that is a PRAM cell can only tolerant limited number of write operations, becomes the main barrier in practical applications. This paper studies the wear reduction techniques of PRAM based FS in H.264 codec system. On the basis of rate-distortion theory, the content oriented selective writing mechanisms are proposed to reduce bit updates in the reference frame buffers. Experiments demonstrate that, for typical video sequences with different frame sizes, our methods averagely achieve more than 30% reduction of bit updates, while introducing around 20% BDBR cost. The power consumption is reduced by 55% on average, and the estimated PRAM lifetime is extended by 61%.**

I. Introduction

High definition video codec requires a high capacity of memory in the video codec system. In the most widely used H.264 Video Codec System, the off-chip storage which mainly used to store the reference frames, is named Frame Store (FS) and has a large capacity. Currently, FS is implemented by the off-chip DRAM. As the frame size get larger and Multiple Reference Frames (MRF) is adopted, the size of FS grow linearly with the video frame size and the number of reference frames. With the feature size of DRAM shrinks, the leakage power of DRAM increases. The high power consumption of DRAM restricts its practical application of high definition codec, especially on mobile devices, of which the size and the power budget are quite limited [1].

To overcome the obstacle of off-chip memory size as well as power consumption, Phase-change Random Access Memory (PRAM) is one possible solution. PRAM is one of the emerging non-volatile memories. As compared with DRAM, PRAM has increased the density by up to 300% [2]. Furthermore, due to the non-volatile nature, PRAM does not need refreshing, and its leakage power is very low. PRAM offers a comprehensive solution to the burgeoning size and power problems of the traditional DRAM storage.

However, the write endurance issue is the critical challenge of replacing DRAM with PRAM. A PRAM cell can only tolerate 10^8 - 10^9 write operations [3]. To push PRAM in the industrial applications, numerous efficient methods for PRAM write reduction have been suggested in literatures [3][4]. Differential write (DR) is one simple but effective scheme, in which the existing data and new data to be written are compared in a bit-by-bit manner, and only the different bits are updated in PRAM [4]. Even employing the differential writing strategy, the updates to PRAM cells are not distributed uniformly, and PRAM lifetime is limited by the most used cell. Wear leveling methods are proposed to distribute writes over PRAM cells in a uniform way [3]. The aforementioned proposals are developed aiming to the general-purpose applications. For video applications, Kwon et al. minimize the number of writes to PRAM by using the lossless compression methods [5].

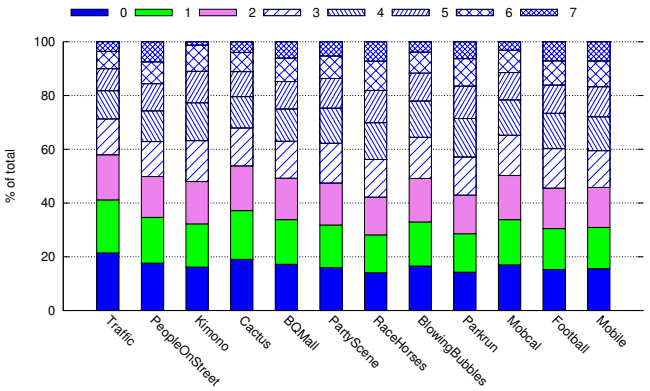

Fig. 1. Write density statistics of each bit in a pixel in reference frame buffer

In H.264 video coding, we notice that each bit of the reference pixels possesses different importance. Because of the temporal locality between neighboring frames and the spatial locality among the nearby pixels in the same picture, the pixels in successive frames with the same coordinate always have the approximate values. In consequence, the least significant bits (LSBs) updates more frequently than the most significant ones (MSBs). To verify this variation, we profiled the updates to each bit inside the reference frame pixels by using JM reference software. Figure 1 shows the statistics. It can be observed that, on average, the least 3 significant bits contributes more than 50% of the bit updates. In contrast, the update of the most 3 significant bits merely accounts for 26% on average. As the ith bit in one pixel has the weight 2^{i-1}, saving the write of LSBs leads to smaller coding quality degradation than MSBs.

In this paper, leveraging on the investigation of texture and motion features of current image block, we propose Content-