Implementation of multi-standard video decoding algorithms on a coarse-grained reconfigurable multimedia processor

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***Abstract*—This paper proposed a THPHP (Task-based Hybrid Parallels and Hybrid Pipelines) scheme to implement multi-standard video decoding algorithms, i.e. MPEG-2, H.264 and AVS (Audio Video coding Standard), on a heterogeneous coarse-grained reconfigurable multimedia processor called REMUS (REconfigurable MUltimedia System). Multiple level parallelism and multiple level pipeline techniques are proposed in this scheme. Simulation results show that the video decoder can support H.264 HP (High Profile) 1920x1080@30fps (frame per second) streams, AVS JP (Jizhun Profile) 1920x1080@39fps streams, and MPEG-2 MP (Main Profile) 1920x1080@41fps streams when exploiting a 200MHz working frequency.**

I. INTRODUCTION

With the multimedia market booming and fast upgrade of video coding standards, there is a potential market demand for the decoder supporting multiple video standards (e.g. MPEG-2[1], H.264[2], AVS[3]), which not only satisfies the requirements of current standards, but also the requirements of various unknown standards in the future. The ASIC (Application Specific Integrated Circuit) solution has very high energy efficiency (i.e. high performance and low power consumption) however with inferior flexibility. While the GPP (General Purpose Processor) solution and the programmable DSP solution have very high flexibility however suffered from relatively poor energy efficiency. It is very difficult to catch up with the rapid evolution of multimedia market by relying on the ASIC, GPP and programmable DSP solutions, or even the combination of them. Currently, reconfigurable system is becoming an attractive topic to fulfill the rigid requirements of the various evolving video standards.

So far, a lot of reconfigurable multimedia systems were proposed, and a lot of mapping and implementation approaches were raised too. [4] proposed a configurable architecture to explore the hardware and software co-design technique for H.264 decoder with task-based MB (Macro-Block) level pipeline and MB-based parallel technique. [4] implemented the reconfiguration by easily adding or deleting accelerator modules, which was more flexible than ASIC, and also more efficient than processor-based solution. However, its reconfiguration was still inferior. [5] mapped H.264 decoder onto ADRES [6], which was a flexible coarse-grained reconfigurable architecture. The overhead of the pipeline operations heavily hampered the performance of some mapped kernels in [5]. [7] implemented H.264 decoding algorithm onto XPP-III [8][9]. [7] could decode H.264 streams with high performance, i.e. 1920x1080@24fps streams at 450MHz working frequency. However, there is no detailed description about the task level scheduling and mapping methods for multi-standard video decoder based on reconfigurable architectures in the above literatures, which has a large impact on the performance of the video decoder.

In this paper, a scheme called THPHP is presented to implement multi-standard (MPEG-2, H.264 and AVS) video decoding on a heterogeneous coarse-grained reconfigurable multimedia processor REMUS [10]. In order to reduce synchronization overhead and improve the decoding performance, multiple level parallelism and multiple level pipeline techniques are proposed.

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